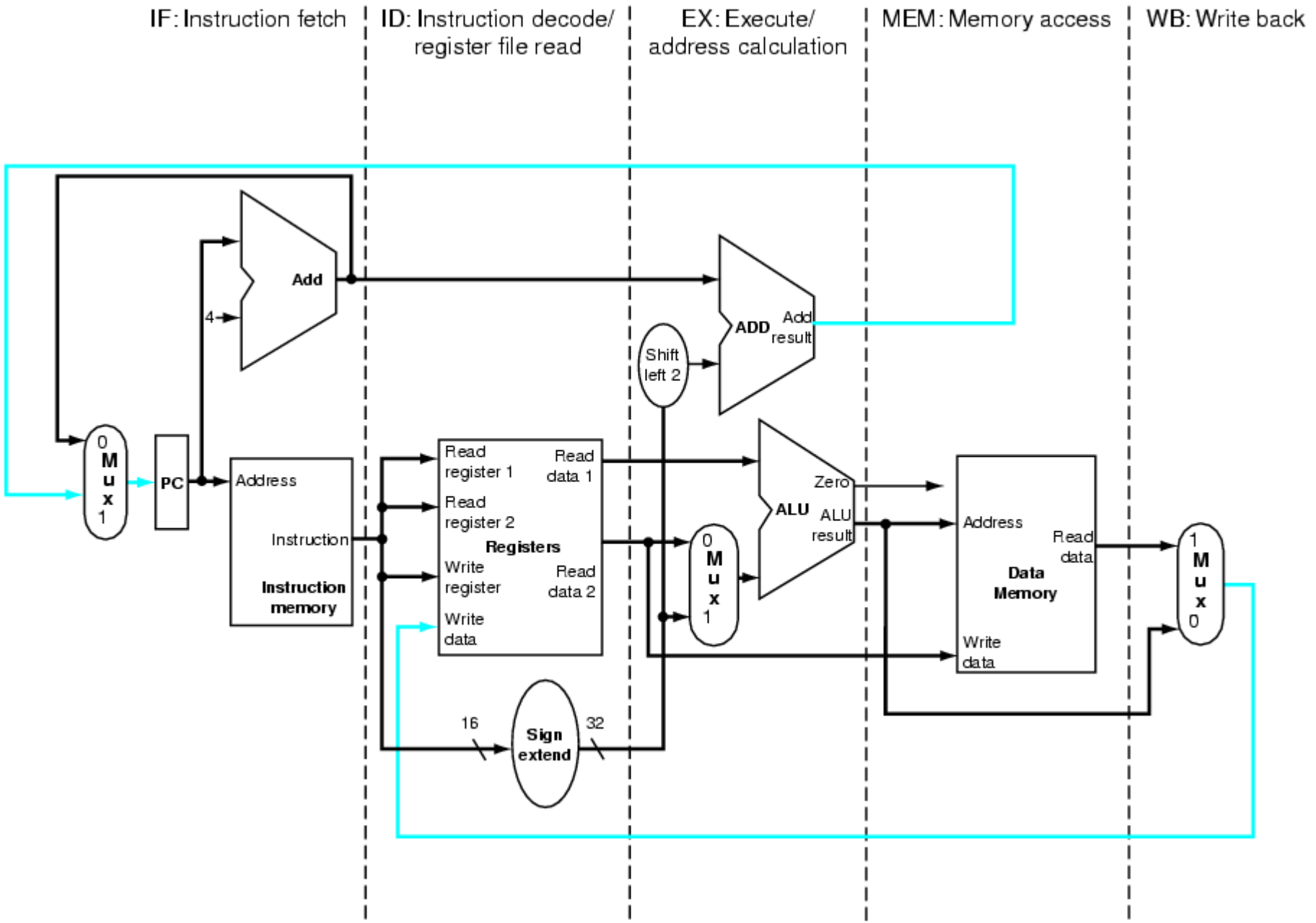
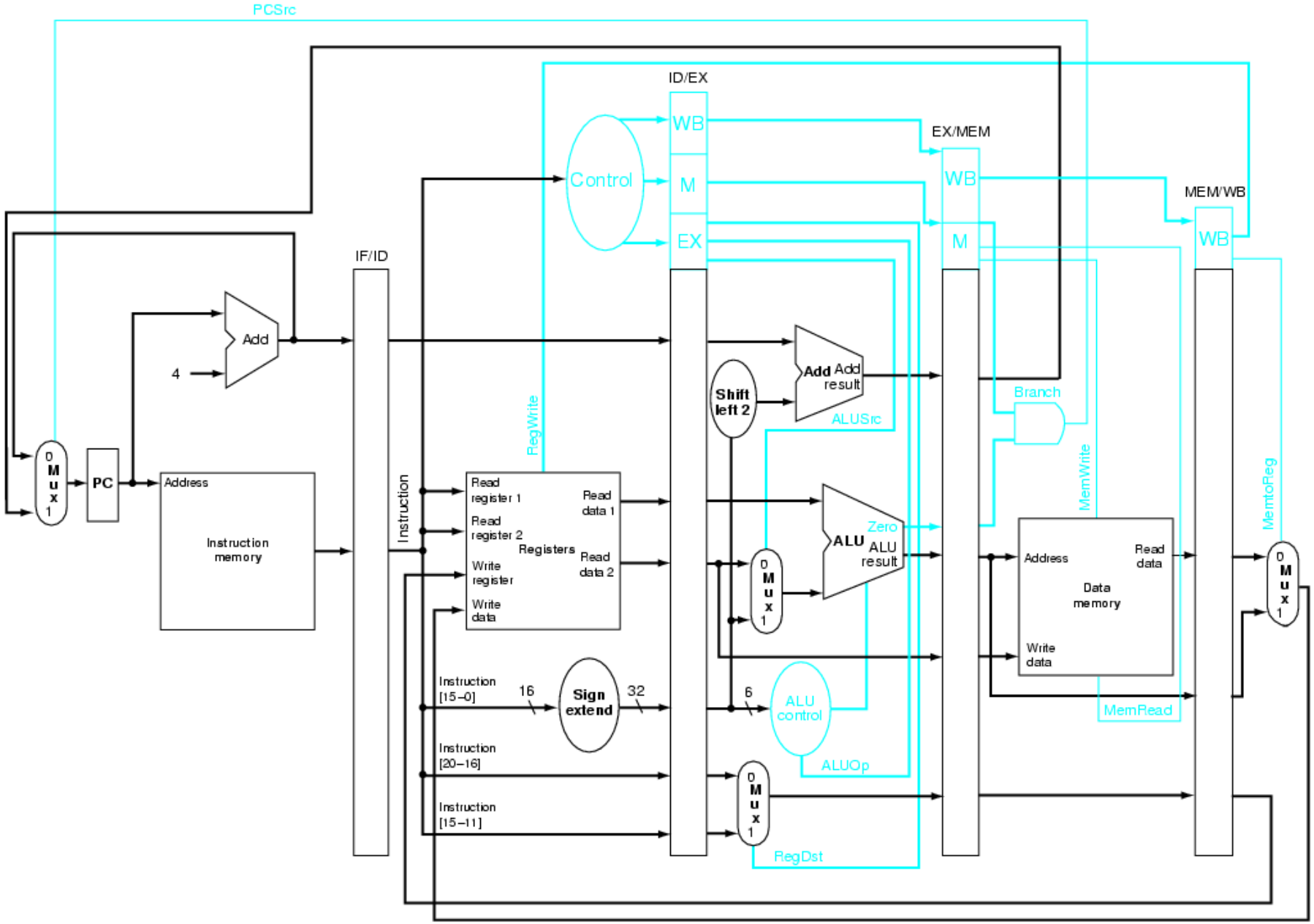
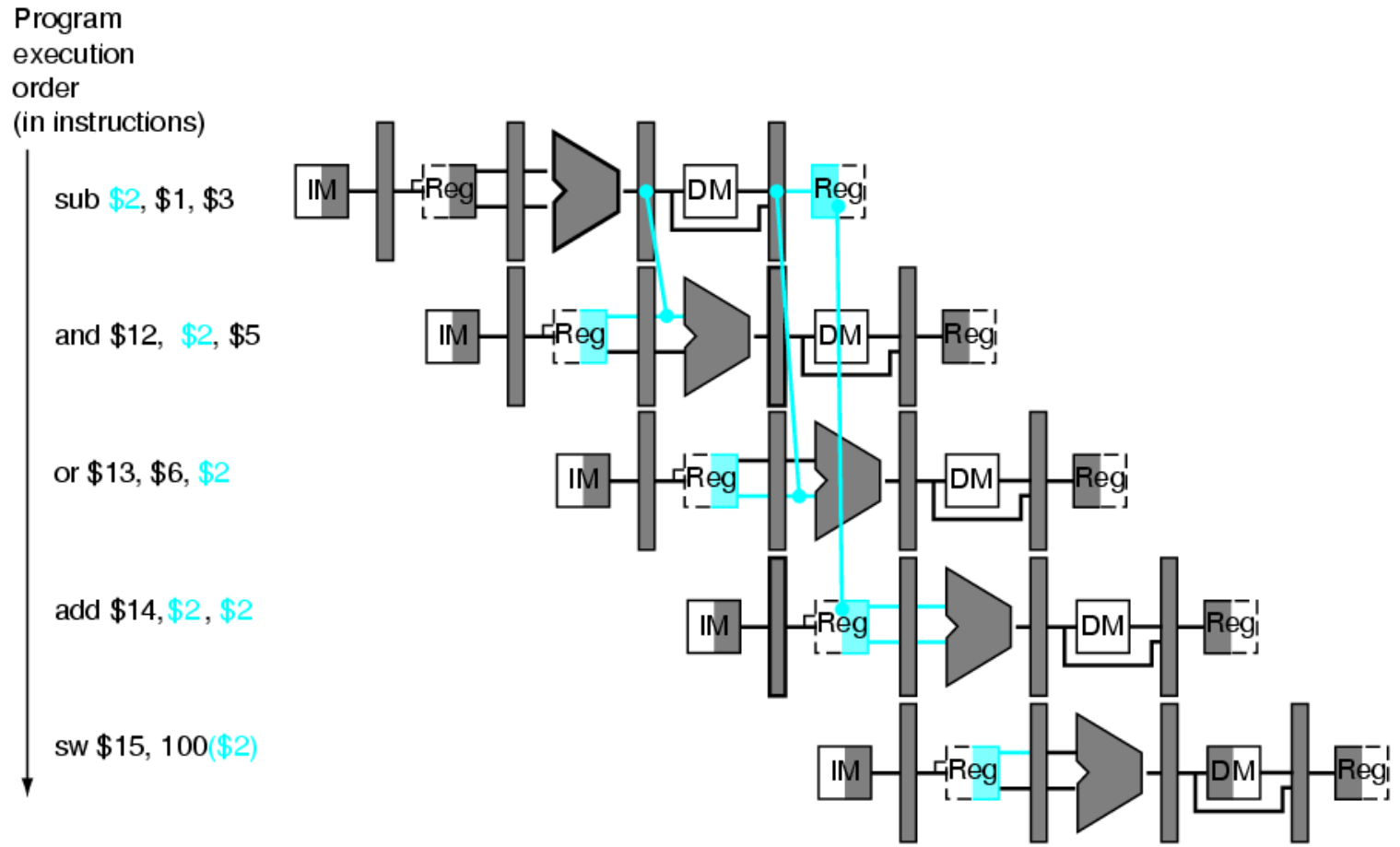

IF: Instruction fetch
ID: Instruction decode/ register file read
EX: Execute/ address calculation
MEM: Memory access
WB: Write back
Add
4
ADD
Add result
Shift left 2
0
M
u
x
1
PC
Address
Instruction
Instruction memory
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
ALU
Zero
ALU result
Address
Read data
Data Memory
Write data
16
Sign extend
32


PCSrc
ID/EX
EX/MEM
MEM/WB
WB
M
EX
Control
IF/ID
Add
4
M
u
x
0
1
PC
Address
Instruction memory
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Instruction [15–0]
16
Sign extend
32
Instruction [20–16]
Instruction [15–11]
Shift left 2
Add
Add result
ALUSrc
ALU
Zero
ALU result
6
ALU control
ALUOp
RegDst
Branch
MemWrite
MemRead
MemtoReg
Address
Read data
Data memory
Write data

Time (in clock cycles)

	CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
Value of register $2:	10	10	10	10	10/–20	–20	–20	–20	–20
Value of EX/MEM:	X	X	X	–20	X	X	X	X	X
Value of MEM/WB:	X	X	X	X	–20	X	X	X	X



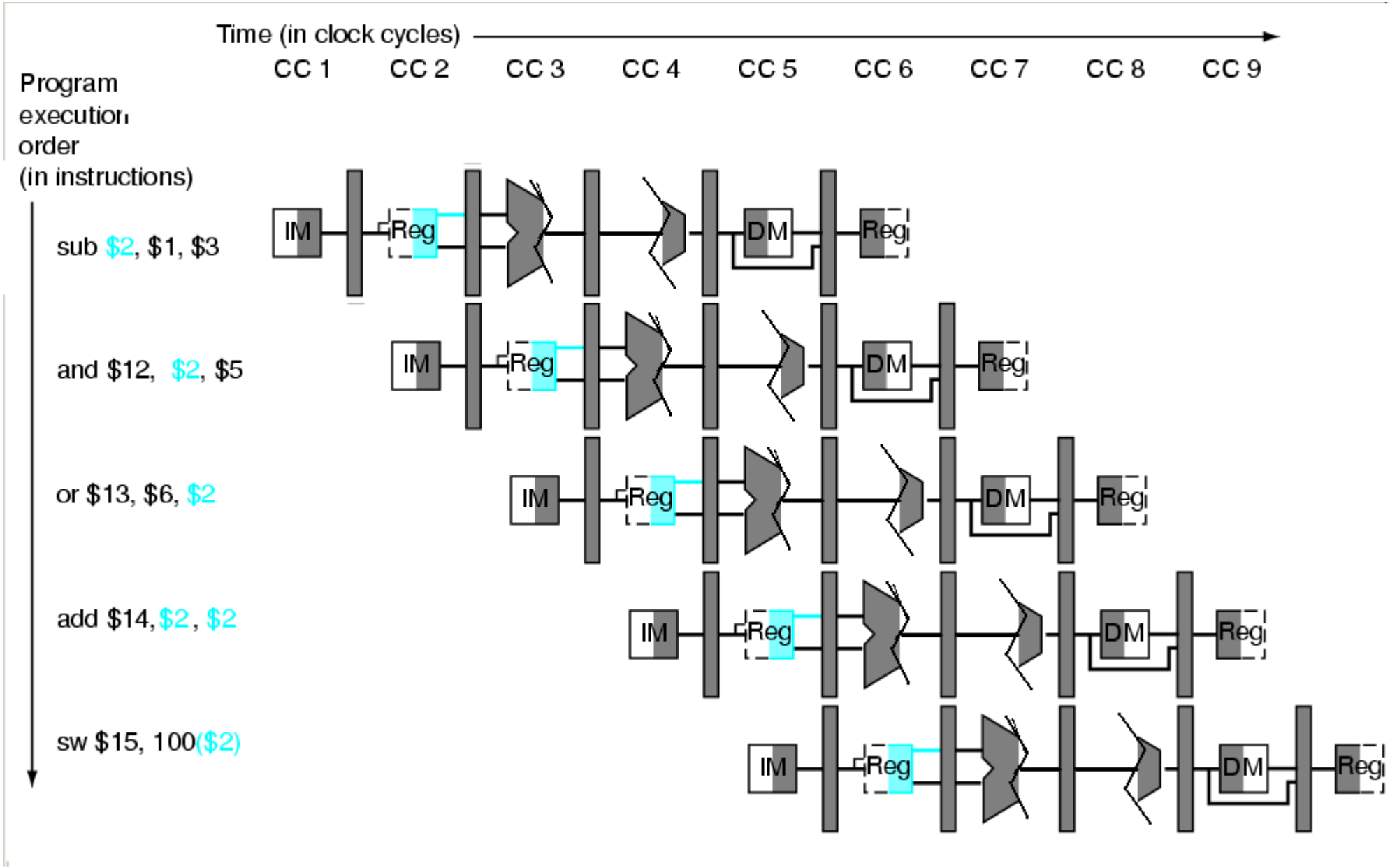
Data Hazards/Forwarding

- Things we can forward
  - ALU result to ALU operand 1 behind
  - ALU result to register read 2 behind (not needed)
  - ALU to Instruction Fetch 3 behind (not data dep.)
  - MemRead to MemWrite 1 behind
  - MemRead to ALU operand 2 behind
  - MemRead to register read 3 behind (not needed)
  - MemRead to Instruction Fetch 4 behind(not data)
- MemRead to register read is just shortcut through register file

Data Hazards

- Things we can't forward remain hazards – so we stall by inserting a bubble
  - MemRead to ALU operand 2 behind
- Bubble – doesn't matter what you do, so long as there are no side effects, such as:
  - write to register
  - write to memory
  - cause an exception
  - read from memory/co-processor register

Extended Pipeline



Next Lab

- Split into two parts
  - Splitting datapath and adding pipeline registers
  - Adding support for Forwarding/Stalling
- First part will only require a check off, no turn-in